Unit: mm

TOSHIBA Transistor Silicon P Channel MOS Type

SSM6J07FU

Power Management Switch High Speed Switching Applications

- · Small package
- Low on resistance
 - : $R_{on} = 450 \text{ m}\Omega \text{ (max) (V}_{GS} = -10 \text{ V)}$
 - : $R_{on} = 800 \text{ m}\Omega \text{ (max) (V}_{GS} = -4 \text{ V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DS}	-30	V	
Gate-source voltage		V_{GSS}	±20	V	
Drain current	DC	I _D	-0.8	А	
	Pulse	I _{DP}	-1.6		
Drain power dissipation		P _D (Note 1)	300	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the

absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.32 mm $^2 \times$ 6)

1, 2, 5, 6 : DRAIN 3 : GATE 4 : SOURCE US6 JEDEC — JEITA — TOSHIBA 2-2J1D

Weight: 6.8 mg (typ.)

Marking

6 5 4 KDF

Equivalent Circuit (top view)

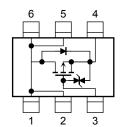
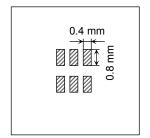


Figure 1: 25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.32 mm² \times 6



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

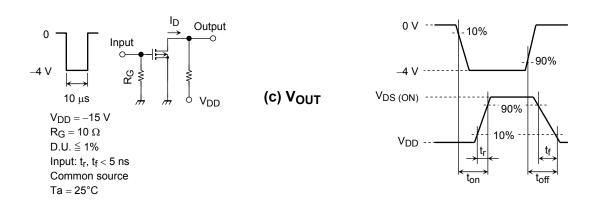
Chara	cteristics	Symbol	Test Condition		Тур.	Max	Unit
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$		_	±1	μА
Drain-source brea	kdown voltage	V (BR) DSS	$I_D = -1$ mA, $V_{GS} = 0$		_	_	V
Drain cut-off curre	nt	I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0$	_	_	-1	μА
Gate threshold vo	Itage	V_{th}	$V_{DS} = -5 \text{ V}, I_D = -0.1 \text{ mA}$	-1.1	_	-1.8	V
Forward transfer a	admittance	Y _{fs}	$V_{DS} = -5 \text{ V}, I_D = -0.4 \text{ A}$ (No	e2) 0.7	_	_	S
Drain-source ON resistance		R _{DS} (ON)	$I_D = -0.4 \text{ A}, V_{GS} = -10 \text{ V}$ (No	e2) —	350	450	mΩ
			$I_D = -0.4 \text{ A}, V_{GS} = -4 \text{ V}$ (No	e2) —	570	800	
			$I_D = -0.4 \text{ A}, V_{GS} = -3.3 \text{ V}$ (No	e2) —	0.7	1.6	Ω
Input capacitance		C _{iss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		130	_	pF
Reverse transfer capacitance		C _{rss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		16	_	pF
Output capacitance		C _{oss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		52	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -15 \text{ V}, I_D = -0.4 \text{ A},$		28	_	ns
	Turn-off time	t _{off}	$V_{GS} = 0 \sim -4 \text{ V}, R_G = 10 \Omega$		38	_	ns

Note 2: Pulse test

Switching Time Test Circuit

(a) Test circuit

(b) V_{IN}

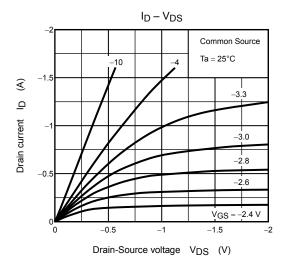


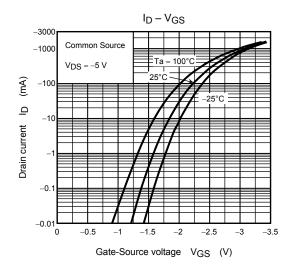
Precaution

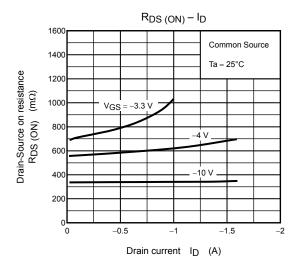
 V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -100~\mu A$ for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} .

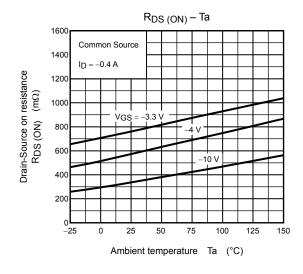
(relationship can be established as follows: V_{GS} (off) $< V_{th} < V_{GS}$ (on)

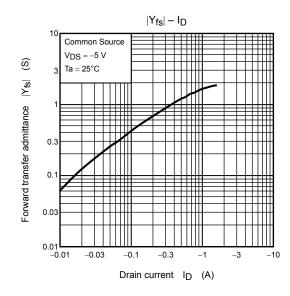
Please take this into consideration for using the device.

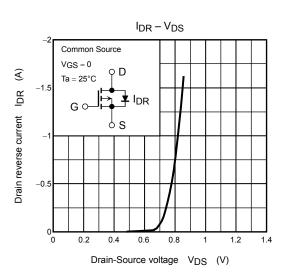


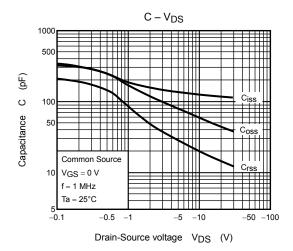


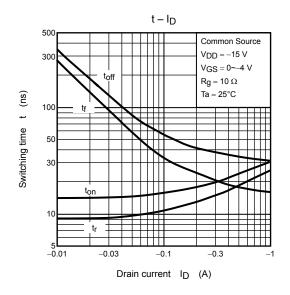


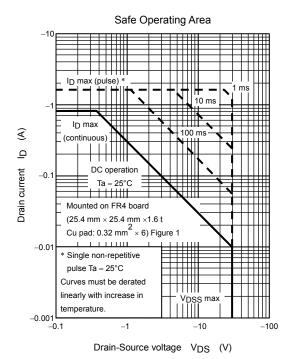


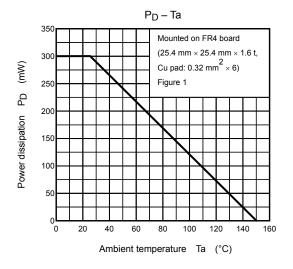












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20070701-EN GENERAL

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